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Docket No. ITL.0202US

In Re Application Of: **Eric C. Hannah, David S. Vannier, And Carol A. Jacobson**

Serial No.	Filing Date	Examiner	Group Art Unit
09/318,684	May 25, 1999	Cas P. Stulberger	2132

Invention: **Digital Video Display System**

#11

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **December 19, 2003**

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#11

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Applicants:	ERIC C. HANNAH, DAVID S. VANNIER, AND CAROL A. JACOBSON	Group Art Unit:	2132
Serial No.:	09/318,684	Examiner:	Cas P. Stulberger
Filed:	May 25, 1999		
For:	DIGITAL VIDEO DISPLAY SYSTEM	Atty. Dkt. No.:	ITL.0202US (P7008)

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APPEAL BRIEF

Sir:

Applicants respectfully appeal from the final rejection mailed September 24, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 009993/0729.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-30. Claims 1-11 and 13-30 are pending. Claims 3-6 are indicated as being allowable (*see* Advisory Action, mailed December 10, 2003). Further, claims 24 and 26 were not rejected under any ground in the Final Office

Action mailed September 24, 2003, and are thus considered to be allowable. Thus claims 1, 2, 7-11, 13-23, 25, and 26-30 are the subject of this appeal.

IV. STATUS OF AMENDMENTS

All amendments entered prior to the Final Office Action have been entered. No amendments have been filed since receipt of the Final Office Action.

V. SUMMARY OF THE INVENTION

A video display system 10, shown in Fig. 1, may include a video display housing 12 coupled to a modular, upgradeable housing or platform 18 by a graphics bus 20. In one embodiment of the present invention, the display hardware is largely contained in the upgradeable platform 18. Thus, the display may be used for an extended time with advances in hardware incorporated by replacing various cards which may be inserted into the slots 22, 24, 26 and 28 in the platform 18. Processed video, in a digital format, is transmitted across the graphics bus 20 to the display housing 12 where it may be shown on the screen 14 and audio may be heard through the speakers 16.

Since the hardware in the display housing 12 may be kept to a minimum, technical advances may be readily incorporated into the video display system without undue cost to the owner and user. For example, the platform 18 may receive a plurality of hot pluggable cards including a motherboard card received in the slot 22 and a plurality of device function cards received in the slots 24 through 28. See Specification, p. 4.

Incoming video may be processed by the platform 18 and transmitted over an encrypted graphics bus 20 to the display housing 12 where the information may be decrypted and displayed. In accordance with one embodiment of the present invention, the encryption algorithm may encrypt a large portion of the information using a basic system with periodic key

changes and periodic use of higher level encryption so that high data transmission rates may be achieved while preventing pirating of the overall video program. See Specification, p. 5.

The digital cathode ray tube (CRT) display housing 12 may receive graphical data for display in a digital format with final analog conversion occurring in the display rather than before transmitting the data over a bus. See Specification, pp. 6-7.

Each slot 22, 24, 26 or 28 in the platform 18 includes a connector 32 with a power plug 34 which supplies power to a card plugged into the slot. As shown in Fig. 3, in one embodiment of the invention, an inter-integrated circuit (I^2C) plug 36, a Universal Serial Bus (USB) plug 38 (USB Specification, Rev. 1.1, published September 23, 1998 at www.usb.org), a 1394B plug 40 and a bus plug 42 are provided. The name 1394B refers to the Institute of Electrical and Electronics Engineers (IEEE) Specification 1394B-1995 which is a hot pluggable, high speed serial bus that operates at speeds at 800 to 3,200 megabits per second. See Specification, p. 9.

Referring now to Fig. 4, an arrangement of the devices in the slots 22-28 is illustrated using the slot 24 as an example. The same types of techniques may be utilized with the other slots. A card 24a may be inserted into the slot 24 so as to contact the connector 24b in the slot 24. The connector 24b may be connected to the connector 22b in the slot 22. The connector 22b may be a Device Bay connector which couples via a USB bus 38a to the motherboard 22a contained in the slot 22. A 1394B bus 40a may also connect to the motherboard 22a as well as an I^2C bus 36a in one embodiment. The graphics bus 65 couples the connector 22b to the motherboard 22a. The motherboard 22a may couple to the display housing 12 via the graphics bus 20. See Specification, p. 10.

Referring now to Fig. 5, the motherboard 22a is shown as being coupled via the graphics bus 20 to the display housing 12 and to the devices 24a, 26a and 28a via the bus 65 which may

include a combination of the signals indicated by the plugs 34, 36, 38 and 40. The motherboard 22a may include a processor 40 coupled to a cache memory 46 and a north bridge 38. The north bridge 48 may in turn be coupled to a bus 52 and a system memory in the form of a random access memory (RAM) 50.

The bus 52 may include an analog TV tuner/capture card. The bus 52 may also couple a peripheral hub 58 which in turn is coupled to an infrared (IR) transceiver 60. The IR transceiver 60 facilitates communication with remote control units to enable to the user to remotely control the overall display system. Thus, the display itself may include no remote control and may be controlled entirely from the platform 18. See Specification, p. 11.

A display rendering device 56 may also be coupled to the bus 52. The display rendering device 56 may provide the necessary conversions for information transmitted to the display 12. In addition, the rendering device 56 may include an encryption/decryption engine 100 which transmits the information to an encryption/decryption engine in the display 12.

The encryption/decryption engine 100 on the motherboard 22a and the encryption/decryption engine 200 in the display 12 may include an encryption engine 100a/200a as shown in Fig. 6 in accordance with one embodiment of the present invention. The encryption engine may include a linear feedback shift register 122 whose output signal is combined, for example, in a logical combination such as an exclusive OR device with a stream 118 made up of color plane data (TP1, TP2, and TP3). The stream 118 may also include control information 115 and a clock signal 117. An encrypted color output signal 124 results from the logical combination of the linear feedback shift register output signal with the incoming color data. See Specification, p. 12.

Referring next to Fig. 7, the linear feedback shift register 122 is shown in more detail. A shift register 130 includes a plurality of cells numbered zero through twenty-three in one embodiment of the present invention. Based on the level of encryption which is desired, more or less cells may be utilized. The cells include a feedback path 146 which goes through a programmable tap register 134. The feedback information is combined in a logic element 128 with an input signal 126. The output of the linear feedback shift register 122 is indicated at 132. The feedback signal on the path 146 is the result of the signals from the cells which have active taps 133.

An input signal 126 causes the linear feedback shift register to generate a pseudorandom bit sequence as the output signal 132. The nature of the output signal is dependent on the input signal and which cells have active taps 133. See Specification, p. 13.

The programmable tap register 134 sets the tap weights and the location of the taps with respect to the cells 0-23. The tap register 134 receives a tap selection input signal 136 which, for example, may be produced by the processor 44 to control the encryption process.

In general, it may be advantageous, in some embodiments of the present invention, to use a relatively simple encryption engine on a frame by frame basis. At desired intervals, the encryption level may be changed by changing the tap selection signal 136. In one embodiment of the present invention, the same encryption values may be utilized for an entire frame of video and then on frame boundaries the encryption settings may be changed. See Specification, p. 14.

Turning next to Fig. 8, the programmable tap register 134, in one embodiment of the present invention, may include the tap logic 142 which receives signals 144 from the cells 130 and a tap memory 138 which receives the tap selection input signal 136. The tap memory 138

may provide the information which selects the weights and the cells which will be added to the feedback loop 146.

Each encryption/decryption engine 100 and 200 may also include a decryption engine 100b and 200b as illustrated in Fig. 9. The decryption engine works essentially in the reverse of the encryption engine, receiving an encrypted signal 124, and processing it through a logic element 148 in combination with the output from a linear feedback shift register 152 to produce a decrypted color output signal 150. See Specification, p. 15.

VI. ISSUES

A. Are Claims 1 and 8-10 Patentable Under 35 U.S.C. § 102(e) Over Lownes?

B. Is Claim 2 Patentable Under 35 U.S.C. § 102(e) Over Lownes?

C. Is Claim 7 Patentable Under 35 U.S.C. § 102(e) Over Lownes?

D. Are Claims 22-23 and 28 Patentable Under 35 U.S.C. § 102(e) Over Lownes?

E. Are Claims 11, 20 and 21 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett?

F. Is Claim 13 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett?

G. Are Claims 15-17 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett?

H. Is Claim 18 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett?

I. Is Claim 19 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett?

J. Is Claim 25 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett?

K. Is Claim 29 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett?

L. Are Claims 14, 27 and 30 Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett In Further View of Warren?

VII. GROUPING OF THE CLAIMS

For purposes of this appeal, the claims do not stand or fall together. For purposes of this Appeal, Applicants have grouped together claims 1 and 8-10; claims 22-23 and 28; claims 11, 20 and 21; claims 15-17; and claims 14, 27, and 30, as set forth above. Claims 2, 7, 13, 18, 19, 25, and 29 are each grouped alone, as set forth above.

VIII. ARGUMENT

A. Claims 1 and 8-10 Are Patentable Under 35 U.S.C. § 102(e) Over Lownes

Claim 1 recites a digital television system including first and second housings; a receiver adapted to receive a digital television signal in the first housing; a digital television display in the second housing; and a digital graphics bus coupled to the receiver in the first housing and the display in the second housing. Claim 1 and dependent claims 8-10 stand rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,137,539 to Lownes.

The rejection is improper. A rejection under 35 U.S.C. § 102 requires that a prior art reference disclose expressly or inherently every limitation contained in a claim. *Rowe v. Dror*, 42 U.S.P.Q.2d 1550 (Fed. Cir. 1997). If any claimed element is absent from the reference, there is no anticipation. *Id.* Further, it is not enough that the prior art reference discloses all the claimed elements in isolation. Rather, as stated by the Federal Circuit, "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). Such showings are lacking here.

With regard to claim 1, Lownes does not disclose, at least, a digital graphics bus coupled to a receiver in a first housing and a display in a second housing. The Examiner contends that the video cassette recorder (VCR) 113 of Lownes (*see* FIG. 1A of Lownes) meets the limitation of a receiver in a first housing. Final Office Action, p. 5. Furthermore, the Examiner contends that IEEE 1394 bus 96 meets the digital graphics bus, contending that the set top box 90 meets the display in a second housing, because it is connected to a display (i.e., display 98 of FIG. 1A of Lownes). *Id.* at pp. 5-6.

This contention is erroneous, as the IEEE 1394 bus of Lownes is not coupled to a display in a second housing. In this regard, the IEEE 1394 bus of Lownes is coupled between VHS 113 (i.e., a VCR) and set top box 90. Neither of these, however, includes a digital television display. That is, a bus coupled to a set top box that is then in turn coupled (in an unknown manner) to a display of a different housing does not anticipate "a digital graphics bus coupled to...said display in said second housing" as recited by claim 1. This is especially so, as the video signal provided from set top box 90 to display 98 of Lownes is an analog signal, not a digital signal, and thus no digital graphics bus exists therebetween. *See* Lownes col. 4, lns. 47-65. For at least this reason, claims 1 and 8-10 are patentable over Lownes, and the rejection should be reversed.

B. Claim 2 Is Patentable Under 35 U.S.C. § 102(e) Over Lownes

Claim 2 depends from claim 1 and further recites that the first housing is part of a modular platform adapted to receive replaceable cards. Claim 2 stands rejected under §102(e) over Lownes. This rejection is improper, at least for the reasons discussed above with regard to claim 1 (*see* VIII.A).

Dependent claim 2 is further patentable as Lownes nowhere discloses that the first housing is part of a modular platform adapted to receive replaceable cards. In this regard, a VCR

is not a "modular platform," and cassette tapes are not "replaceable cards". This is so, at least because Lownes nowhere discloses that the VCR is a modular platform or that it receives replaceable cards. For these further reasons, claim 2 is patentable and the rejection should be reversed.

C. Claim Is 7 Patentable Under 35 U.S.C. § 102(e) Over Lownes

Claim 7 depends from claim 6 (which is indicated to be allowable, *see* Advisory Action, mailed December 10, 2003, p. 2) and further recites that a replaceable card in the first housing is a digital video disk card. Claim 7 stands rejected under §102(e) over Lownes. For the same reasons discussed above regarding claim 1 (*see* VIII.A), claim 7 is patentable.

Dependent claim 7 is further patentable, as nowhere does Lownes disclose a replaceable card that is a digital video disk card.

Claim 7 is further patentable, as it depends from claim 6, which itself is indicated to be allowable. Thus the rejection should be reversed.

D. Claims 22-23 and 28 Are Patentable Under 35 U.S.C. § 102(e) Over Lownes

Claim 22 recites a modular platform for a digital television system that includes a housing having a plurality of slots, each including a plug adapted to removably receive a card; a bus electrically coupling the slots to one another; and each of the plugs are adapted to receive more than one type of serial bus interface. Claim 22 and claims 23 and 28 depending therefrom stand rejected under §102(e) over Lownes. This rejection is improper.

First, Lownes does not disclose a modular platform. That is, nowhere does Lownes disclose that any of its VCR, set top box or display form a modular platform. Nor does Lownes disclose a housing including a plurality of slots each including a plug adapted to removably receive a card, and certainly not where each of the plugs are adapted to receive more than one

type of serial bus interface. Instead, the VCR, set top box and display of Lownes are simply the standard devices of the prior art. For at least these reasons, claims 22, 23 and 28 are patentable over Lownes, and the rejection should be reversed.

E. Claims 11, 20 and 21 Are Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett

Independent claim 11 recites a digital graphics bus to couple a digital television receiver and display and which includes an encryption engine coupled to the bus to encrypt signals transferred from the receiver to the bus, which may be provided at two different levels of encryption; and a decryption engine coupled to the bus to decrypt signals transferred from the bus to the display.

Claims 11, 20, and 21 stand rejected under §103(a) over Lownes in view of Tsukamoto and further view of U.S. Patent No. 5,784,427 (Bennett). This rejection is improper as there is no motivation to combine Lownes or Tsukamoto with Bennett, which relates to a feedback and shift unit, and not a digital graphics bus or a modular platform for digital television systems. This is especially so, as the shift unit of Bennett is in a digital signal processor for a GSM (i.e., wireless) communication system.

Furthermore, neither Lownes or Tsukamoto teach or suggest an encryption engine that provides two different levels of encryption. Nor does Bennett. Instead, Bennett merely discloses a linear feedback shift register that may be used for purposes of encryption/decryption of wireless communications. However, nowhere does Bennett teach or suggest that such encryption may be provided at two different levels. For at least these reasons, claims 11 and 20-21 are patentable over the proposed combination and the rejection should be reversed.

F. Claim 13 Is Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett

Claim 13 depends from claim 11 and further recites that the bus is adapted to periodically encrypt at a higher level of encryption. Dependent claim 13 stands rejected under §103(a) over Lownes in view of Tsukamoto and in further view of Bennett. For the same reasons discussed above regarding claim 11 (*see* VIII.E), the rejection is improper.

Furthermore, nowhere does Bennett teach or suggest periodically encrypting at higher level of encryption. That is, while Bennett may disclose encryption, nowhere does Bennett teach or suggest that an encryption level may be changed periodically, as recited by claim 13. For this further reason, claim 13 is patentable and the rejection should be reversed.

G. Claims 15-17 Are Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett

Dependent claim 15 depends from claim 11 and further recites that the encryption/decryption engines include linear feedback shift registers. Claim 15 and claims 16 and 17 depending therefrom stand rejected under §103(a) over Lownes in view of Tsukamoto and Bennett. For at least the same reasons discussed above with regard to claim 11 (*see* VIII.E), claim 15 is patentable.

Claim 15 is further patentable, as there is no motivation to combine the linear feedback shift registers of Bennett with either of Tsukamoto or Lownes. In this regard, the Examiner irrefutably appears to have merely engaged in the hindsight-based obviousness analysis that has been widely and soundly disfavored by the Federal Circuit. In order to prevent a hindsight-based obviousness analysis, the Federal Circuit has held "to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion

or teaching of the desirability of making the specific combination that was made by the applicant." *In re Kotzab,* 55 U.S.P.Q.2d 1313, 1316-17 (Fed Cir. 2000).

With respect to claim 15, the Final Office Action contains no factual support for motivation or the manner in which Lownes, Tsukamoto, and Bennett must be modified to render obvious claim 15. Conclusory statements that "it would have been obvious...to combine the digital television of the Lownes with the linear feedback shift registers and tap registers of Bennett in order to reduce a minimum the number of processing steps required in a processor" (Final Office Action, p. 8) do not adequately set forth a proper motivation to combine. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2001).

Because the Examiner entirely fails to adduce any factual findings that would support, even inferentially, a motivation for, or suggestion of, the alchemy by which Lownes, Tsukamoto, and Bennett might be modified to yield the subject matter of claim 15, a *prima facie* case of obviousness has not been made. Accordingly, claim 15 and claims 16 and 17 depending therefrom are patentable, and the rejection should be reversed.

H. Claim 18 Is Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett

Claim 18 depends from dependent claim 17 and further recites a combiner adapted to combine a seed signal together with feedback from a programmable tap register to create an input signal to the linear feedback shift register. Claim 18 stands rejected under §103(a) over Lownes in view of Tsukamoto and Bennett. This rejection is improper, at least for the reasons discussed above with regard to claims 11 and 15 (*see* VIII.E and VIII.G), from which claim 18 depends.

Dependent claim 18 is further patentable as neither Bennett nor the other cited references teach or suggest a combiner adapted to combine a seed signal together with feedback from a

programmable tap register. In this regard, the input sequence injected into a shift register shown in FIG. 3 of Bennett and referred to by the Examiner (Final Office Action, page 7) does not teach or suggest a combiner that combines a seed signal and feedback from a programmable tap register. Thus the rejection should be reversed.

I. Claim 19 Is Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett

Claim 19 depends from claim 18 and further recites that the tap register includes combinatorial logic and tap memory. Claim 19 stands rejected under §103(a) over Lownes in view of Tsukamoto and Bennett. This rejection is improper, at least for the reasons discussed immediately above regarding claim 18 (*see* VIII.H).

Claim 19 is further patentable, as Bennett does not teach or suggest a tap register that includes combinatorial logic and tap memory. In this regard, the memory of FIG. 11 of Bennett referred to by the Examiner (Final Office Action, page 7) is not included in a tap register; nor is it combinatorial logic. Thus claim 19 is patentable and the rejection should be reversed.

J. Claim 25 Is Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett

Claim 25 depends from independent claim 22 and further recites that the encryption engine is adapted to encrypt at two different levels of encryption. For at least the reasons discussed above regarding claim 11 (*see* VIII.E), claim 25 is patentable, as none of the references teach or suggest encryption at two different levels.

Furthermore, claim 25 is further patentable because none of the references teach or suggest a housing having a plurality of slots each including a plug to removably receive a card in which each of the plugs is adapted to receive more than one type of serial bus interface, as recited by claim 22 from which claim 25 depends.

K. Claim 29 Is Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett

Claim 29 is an independent claim and recites a method including providing a receiver in a first housing for receiving a digital television signal; providing a display in a second housing coupled to the first housing; transmitting encrypted video signals between the housings; and periodically changing the level of encryption of the signals. Claim 29 stands rejected under §103(a) over Lownes in view of Tsukamoto and in further view of Bennett. This rejection is improper.

First, as discussed above regarding claim 11 (*see* VIII.E), there is no motivation to combine Lownes, Tsukamoto and Bennett. Second, there is no teaching or suggestion in any of the references for periodically changing a level of encryption of the digital signals. This is so, as nowhere does Bennett or the other references teach or suggest periodically changing encryption levels (*see* VIII.F). Thus for this further reason, claim 29 is patentable and the rejection should be reversed.

L. Claims 14, 27 and 30 Are Patentable Under 35 U.S.C. § 103(a) Over Lownes In View of Tsukamoto and In Further View of Bennett In Further View of Warren

Claim 14 depends from claim 13 (which itself depends from claim 11) and further recites that the level of encryption is adapted to change on frame boundaries. Claims 14, 27 and 30 stand rejected under § 103(a) over Lownes in view of Tsukamoto in view of Bennett in further view of U.S. Patent No. 5,969,909 (Warren). For at least the same reasons discussed above regarding claims 11 and 13 (*see* VIII.E and VIII.F), claim 14 is patentable.

The rejection of the above claims is further improper, as there is no motivation or suggestion to combine these four references. In this regard, the Final Office Action is totally deficient of any motivation to combine the references. Instead, the Final Office Action merely

conclusorily states that "it would have been obvious...to combine the encryption method as disclosed in Lownes with the method of changing the key as disclosed in Warren in order to provide for electronic copy management of various forms of multi-media... ." Final Office Action, pp. 8-9. This conclusory contention does not provide the requisite motivation. *See In re Kotzab,* 55 U.S.P.Q.2d at 1316-1317. Furthermore, the contention is incorrect, as Lownes does not even disclose encryption. Further, Warren does not teach or suggest changing encryption levels on frame boundaries. Instead, Warren only teaches that encryption keys may be different on different frames; there is no teaching or suggestion to change encryption levels on frame boundaries.

Thus claims 14, 27 and 30 are patentable and the rejection should be reversed.

IX. CONCLUSION

Since the rejections of the claims are baseless, they should be reversed.

Respectfully submitted,

Date: 2/17/04

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APPENDIX OF CLAIMS

The claims on appeal are:

1. A digital television system comprising:

a first and second housing;

a receiver, adapted to receive a digital television signal, in said first housing;

a digital television display in said second housing; and

a digital graphics bus coupled to said receiver in said first housing and said display in said second housing.

2. The system of claim 1 wherein said first housing is part of a modular platform adapted to receive replaceable cards.

3. The system of claim 2 wherein each of said cards is received in a plug, said plugs for said cards coupled by a bus.

4. The system of claim 1 wherein said graphics bus is coupled to an encryption and a decryption engine so that traffic across said bus may be encrypted.

5. The system of claim 2 wherein one of said cards is a motherboard including a processor.

6. The system of claim 5 wherein another of said cards is a television tuner/capture card.

7. The system of claim 6 wherein one of said cards is a digital video disk card.

8. The system of claim 2 including plugs in said platform for both power and data.

9. The system of claim 8 wherein said plugs are adapted to receive two different types of serial bus interfaces.

10. The system of claim 2 wherein said platform includes a processor and an infrared interface.

11. A digital graphics bus to couple a digital television receiver and a digital television display comprising:

a encryption engine coupled to said bus to encrypt signals transferred from said receiver to said bus, said encryption engine to provide two different levels of encryption; and

a decryption engine coupled to said bus to decrypt signals transferred from said bus to said display.

13. The bus of claim 11 wherein said bus is adapted to periodically encrypt at a higher level of encryption.

14. The bus of claim 13 wherein the level of encryption is adapted to change on frame boundaries.

15. The bus of claim 11 wherein said encryption and decryption engines include linear feedback shift registers.

16. The bus of claim 15 wherein said shift registers include programmable tap registers.

17. The bus of claim 16 wherein said programmable tap registers are adapted to receive external tap selection input signals.

18. The bus of claim 17 including a combiner adapted to combine a seed signal together with feedback from said programmable tap register to create an input signal to said linear feedback shift register.

19. The bus of claim 18 wherein said tap register includes combinatorial logic and tap memory.

20. The bus of claim 11 including a decryption and an encryption engine on both ends of said bus.

21. The bus of claim 11 wherein said bus is adapted to transfer streaming video at 100 megahertz or higher.

22. A modular platform for a digital television system comprising:

a housing including a plurality of slots, each slot including a plug adapted to removably receive a card;

a bus electrically coupling said slots to one another; and

each of said plugs adapted to receive more than one type of serial bus interface.

23. The platform of claim 22 wherein one of said slots is coupled to receive a motherboard with a processor.

24. The platform of claim 22 including a encryption and decryption engine coupled to an external bus.

25. The platform of claim 24 wherein said encryption engine is adapted to encrypt at two different levels of encryption.

26. The platform of claim 25 wherein said encryption levels are changed periodically.

27. The platform of claim 26 wherein said encryption levels are changed on frame boundaries.

28. The platform of claim 22 wherein said plugs are adapted to receive both data and power connections.

29. A method of implementing a digital television system comprising:

providing a receiver in a first housing for receiving a digital television signal;

providing a display in a second housing coupled to said first housing;

transmitting encrypted video signals between said housings; and

periodically changing the level of encryption of said signals.

30. The method of claim 29 wherein changing the level of encryption includes changing the level of encryption on frame boundaries.